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Asynchronous HVDC System -based on Three Level NPC Converter

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***Abstract*— Voltage Source Converter High Voltage Direct Current (VSC-HVDC) systems have the ability to rapidly control the transmitted active power and independently exchange reactive power with transmissions systems. The present work investigates the modeling and control design of a high-voltage direct current (HVDC) transmission system based on three-level NPC multilevel converters with Subharmonic PWM modulation technique (SH-PWM), and a feed-forward decoupled current control strategy. By using this control strategy, not only the active and reactive power of HVDC can be controlled independently but also the dynamic responded time can be shortened. Simulation studies of a 200MW/ ±100 kV back to back VSC-HVDC system connecting two asynchronous ac networks are presented to confirm the satisfactory performance of the proposed system under active and reactive power variations from single phase to ground and three phases to ground fault conditions.**

***Keywords*— NPC multilevel converter, VSC based HVDC, SH-PWM**

I. INTRODUCTION

Voltage Source Converter (VSC)-based High-Voltage Direct Current (HVDC) schemes using insulated-gate bipolar transistors (IGBTs) (known as VSC transmission) has attracted increasing attention. The main advantage of VSC power transmission is the high controllability, the ability to control independently active and reactive power at each terminal and the possibility for linking with dead networks. These characteristics make VSC transmission attractive in many applications like the emerging interconnection with renewable energy sources. The disadvantages are known as higher power losses and higher capital cost compared with conventional HVDC [1-2]. In order to maximize the potential of VSC transmission systems, a number of technology breakthroughs are required. One requirement is the reduction of the power losses and the harmonic distortion generated by the converters. This will allow the reduction of cooling needs and space requirements as well as increasing the system's operating efficiency and reliability. The other one is to ensure that the system operates satisfactorily during abnormal conditions, such as during severe network unbalances.

Theoretically, one promising way forward could be the adoption of a multilevel converter as a building block for the system. There are a number of distinct multilevel converter topologies which have been used or proposed for the VSC transmission system, namely, the neutral-point clamped (NPC), the flying-capacitor (FC) converter, and the cascaded Converters. While these multilevel converters have their respective merits and shortcomings, the selection of the converter topology is a detailed engineering design exercise. It needs to take into account a number of parameters, including the system design and control, power loss, cost, etc… [3]. Due to these characteristics this paper present the element of an asynchronous back-to-back VSC-HVDC system which uses three level neutral point clamped inverter topology with (SH-PWM) technique and a current-control strategy in rotation frame that the ac current is feedforward decoupled made the active and reactive power exchange controlled independently. The simulation results got from MATLAB software confirm that the control strategy provides satisfactory response and strong stability.

II. INVERTER TOPOLOGY

Fig 1 illustrates the fundamental building block of a diode -clamped inverter. In this circuit, the dc-bus voltage is split into three levels by two series-connected bulk capacitors, C_1 and C_2 . The middle point of the two capacitors n can be defined as the neutral point. The inverter in Fig. 1 provides a three-level output across a and n.

$$V_{an} = \left(V_{dc}/2\right), 0, \left(-V_{dc}/2\right)$$

For voltage level $\left(V_{dc}/2\right)$, switches S_{11} and S_{21} need to be turned 'ON'.

For $\left(-V_{dc}/2\right)$ switches $S_{11}^{'}$ and $S_{21}^{'}$ need to be turned 'ON'; and for the '0' level, either pair $\left(S_{21}, S_{11}^{'}\right)$ needs to be turned 'ON'.

The same switching pattern applies across the phase 'b' leg (if 'a' is replaced by 'b') but phase shifted by 180° for

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the single phase configuration (in the three-phase configuration the shifts between the phases will be 120˚) [3].

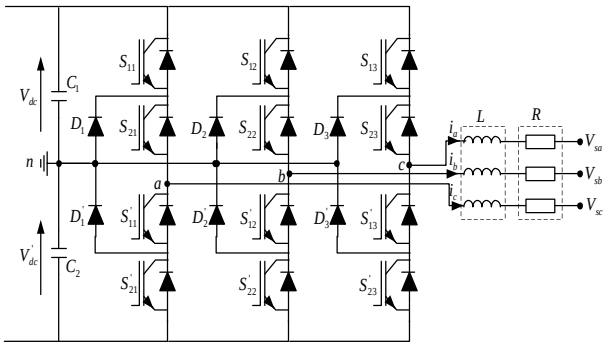

Fig. 1. Basic Model of VSC (Three-Level Neutral Point Clamped inverter circuit topology).

The control strategies are based on reducing harmonic distortion, power losses and speeding transient response. In which, the fundamental frequency switching method and PWM techniques show great advantages. Many different approaches of PWM techniques for multilevel inverters have been published. This paper proposes the Sub-Harmonic PWM (SH-PWM) technique [4], [5], [6].

The control principle of the SH-PWM method is to use several triangular carrier signals keeping only one modulating sinusoidal signal. For the three level inverter, two triangular carriers are needed (generally speaking, if a N-level inverter is employed, N-1 carriers will be needed). The carriers have the same frequency and the same peak-to-peak amplitude, and are disposed so that the bands they occupy are contiguous. The zero reference is placed in the middle of the carrier set.

Fig 2 show an example of the SH-PWM method used for three level inverter.

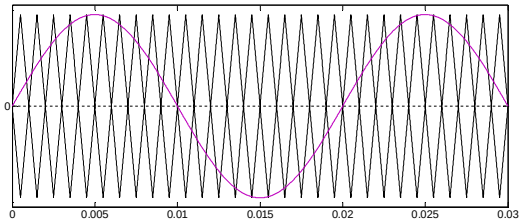

Fig. 2.a. Carrier and modulation waveforms using SH-PWM.Clamped inverter circuit topology).

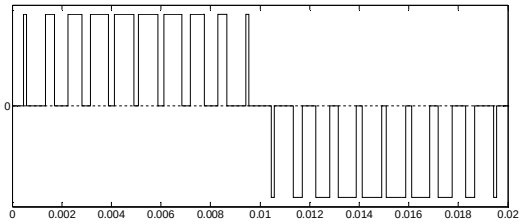

Fig. 2.b. Output voltage waveform using SH-PWM.

III. VSC Transmission Analysis And Control

An equivalent system model for the back- to- back HVDC based on VSC converter is given in Fig. 3. There are two converter stations in the system. Each station shown in Fig. 1 is coupled with ac network via equivalent impedances $Z_1 = Z_{ac1} + Z_{T1}$ and $Z_2 = Z_{ac2} + Z_{T2}$, where Z_{ac1} and Z_{ac2} are the impedances of ac lines, respectively. Z_{T1} and Z_{T2} are the impedances of transformers. dc capacitor $C = C_1 = C_2 = C_1' = C_2'$ is used across dc side of the VSC-HVDC system.

The sending and the receiving VSC stations have same topology structure; we can establish the same model for both. To describe the mathematical models of converter it is assumed that the switches at the converter bridge should not be turn-on at the same time. We define the switch function S_a, S_b and S_c, with S_i the switching function defined by :

$$S_i = \begin{cases} 1 \textit{ upper switch ON} \\ 0 \textit{ bottom switch ON} \end{cases}$$

The mathematical model for the VSC used switch function is [7], [8]:

$$\begin{cases} L\dfrac{di_a}{dt} = -Ri_a + V_{sa} - \left(\dfrac{2S_a - (S_b + S_c)}{3}\right)V_{dc} \\ L\dfrac{di_b}{dt} = -Ri_b + V_{sb} - \left(\dfrac{2S_b - (S_a + S_c)}{3}\right)V_{dc} \\ L\dfrac{di_c}{dt} = -Ri_c + V_{sc} - \left(\dfrac{2S_c - (S_a + S_b)}{3}\right)V_{dc} \\ C\dfrac{dV_{dc}}{dt} = S_a i_a + S_b i_b + S_c i_c - i_{dc} \end{cases} \quad (1)$$

S_a, S_b, S_c are discrete functions. It is difficult to directly analyse the control model. Omitting the high-frequency proportion, we get the steady fundamental frequency component V_{ra}, V_{rb}, V_{rc} to present the VSC output voltage.

The voltage vector equation is:

$$L\frac{di_{abc}}{dt} = -Ri_{abc} + V_{sabc} - V_{rabc} \quad (2)$$

$$\begin{cases} L\dfrac{di_q}{dt} = -Ri_q - \omega Li_d + V_{sq} - V_{rq} \\ L\dfrac{di_d}{dt} = -Ri_d + \omega Li_q + V_{sd} - V_{rd} \end{cases} \quad (3)$$

The current equation of the VSC station is given by:

$$C\frac{dV_{dc}}{dt} = S_q i_q + S_d i_d - i_{load} \quad (4)$$

A. Decoupled system

Formula (4) show that there exist coupling between two axis components, However, the PI current controllers have

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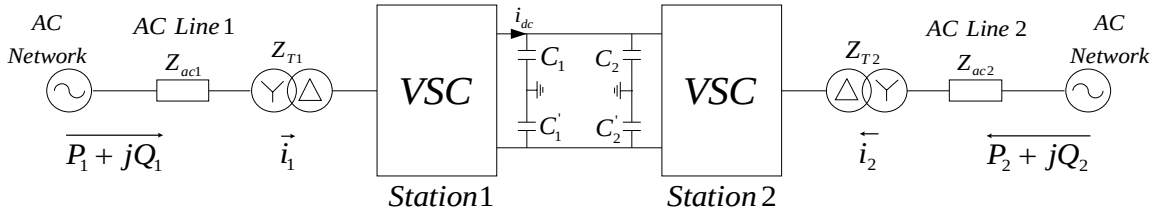

Fig. 3. A physical model for the VSC-HVDC system.

no satisfactory tracking performances when they have to regulate coupled systems. Therefore, in order to improve the performances of the PI current controllers in such systems, cross-coupling terms and voltage feed forward is usually used [9]. Now, assume that the VSC output voltage is determined by the following PI controller:

$$\begin{cases} V_{rq} = -\left(K_{pq} + \dfrac{K_{iq}}{s}\right)\left(i_q^* - i_q\right) - \omega L i_d + V_{sq} \\ V_{rd} = -\left(K_{pd} + \dfrac{K_{id}}{s}\right)\left(i_d^* - i_d\right) + \omega L i_q + V_{sd} \end{cases} \quad (5)$$

Substituting (6) into (4) the control variable equations given by:

$$\begin{cases} L\dfrac{di_q}{dt} = -\left[R - \left(K_{pq} + \dfrac{K_{iq}}{s}\right)\right] i_q - \left(K_{pq} + \dfrac{K_{iq}}{s}\right) i_q^* \\ L\dfrac{di_d}{dt} = -\left[R - \left(K_{pd} + \dfrac{K_{id}}{s}\right)\right] i_d - \left(K_{pd} + \dfrac{K_{id}}{s}\right) i_d^* \end{cases} \quad (6)$$

The structure of the VSC output voltage implemented in the synchronous reference frame is presented in Figure 4:

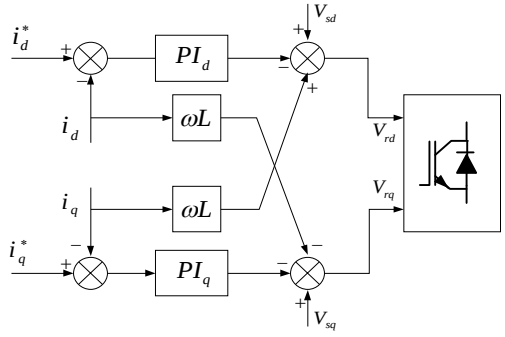

Fig. 4. Decoupled Controller

In dq frame, equation (8) will be:

$$V_{sq} = V_{moy} \quad V_{sd} = 0 \quad (7)$$

So, the active and reactive powers are given by:

$$\begin{cases} P_s = \dfrac{3}{2} V_{sq} i_q + \dfrac{3}{2} V_{sd} i_d = \dfrac{3}{2} V_{sd} i_q \\ Q_s = \dfrac{3}{2} V_{sq} i_d - \dfrac{3}{2} V_{sd} i_q = -\dfrac{3}{2} V_{sd} i_d \end{cases} \quad (8)$$

B. Capacitor voltage and current control

The goal of the dc voltage controller is to regulate the dc-link voltage to its reference and outputs the appointed reactive power to grid. At the dc side, the capacitance holds out the dc bus voltage and the dc cable or line is the channel to flow active power. The exchange of active power between the ac system and the VSC will result in variation of dc-link voltage of the converters. If the ac system provides more real power than the load demand and the converter losses, the excess power will be absorbed by the VSC resulting in the dc-link capacitor voltage to increase. If this real power is less than the load demand and the converter losses, the dc-link capacitor voltage will decrease. It is important to maintain the voltage across the capacitor to ensure continuous power flow. The ac active power current, used for controlling the balance of the dc power, consists of two parts: one is the steady portion, the other is variable portion to compensate the dc voltage fluctuation. This, of course, yields a stationary error in the dc bus voltage, proportional plus integral PI controllers are employed to control the ac side current, and generate references for the ac active power current in the rotation (dq) frames. In these control schemes, the output dc voltage is controlled by an outside voltage loop. The inside feedforward decoupled PI current regulators ensure that the input ac currents track these reference. The dc bus voltage controller is represented in figure (5).

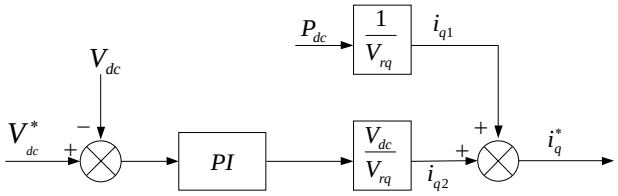

FIG. 5. DC BUS VOLTAGE CONTROLLER FOR VSC-HVDC

When the dc voltage is fixed, the fixed dc current control mode actually controls the active power transmission direction and quantity. The fixed dc bus current controller for the converter is show in figure (6).

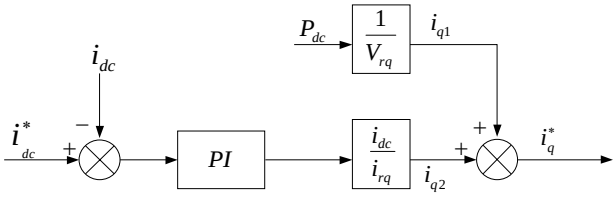

Fig. 6. dc bus Current Controller for VSC-HVDC

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It has the similar control structure to the fixed dc voltage control. PI regulators are also employed to control the ac side active power current. The output dc current is controlled by an outside current loop. The inside feedforward decoupled PI current regulators ensure that the input ac currents track these references [9].

The other aim of the fixed dc voltage and current control is to output the exact reactive power to ac grid as it's needed.

C. Fixed AC bus Voltage Control

In the VSC-based HVDC transmission systems, another variable which can be subject to control is the AC voltage, the control scheme aim to keep the ac bus voltage at the appointed voltage through controlling the VSC station reactive power output. To passive ac net, the ac bus voltage is key to load normal working, the VSC station provide the active power and the reactive power according to the load to hold the ac bus voltage needed.

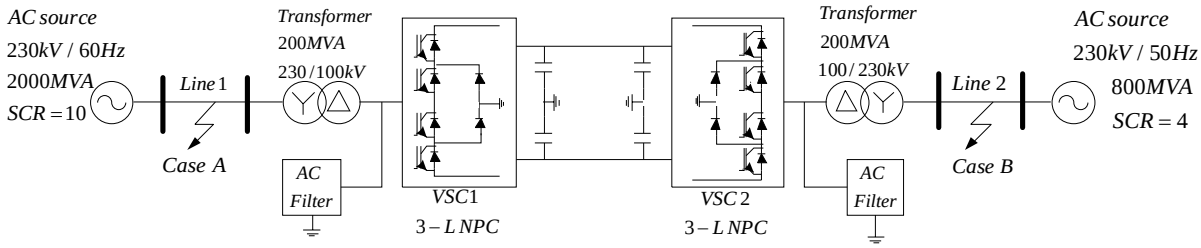

Fig. 7. dc bus Current Controller for VSC-HVDC

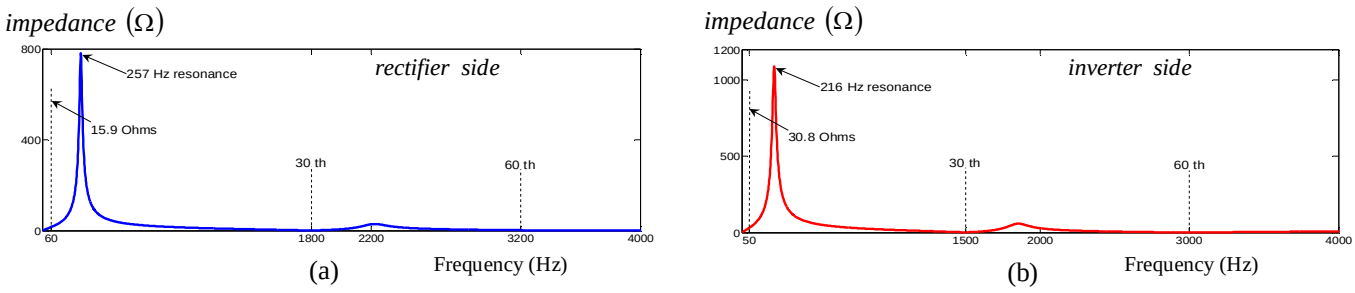

Fig. 8.1. Impedances of the two ac networks

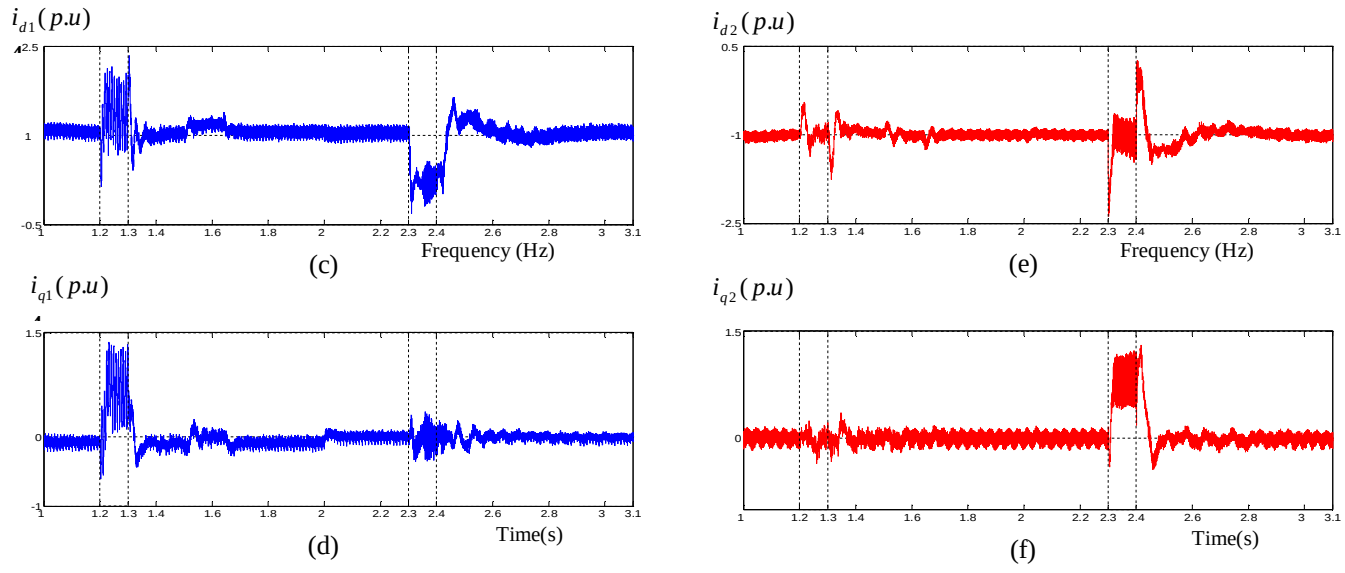

Fig. 8.2. Current control results: (c)-(d) Converter current control responses in dq frame reference (Rectifier side) . (e)-(f) Converter current control responses in dq frame reference (inverter side).

D. System Under Study

An Asynchronous back-to-back HVDC link based on VSC converters rated at 200 MVA (+/- 100 kV) employing three-level NPC converters using close IGBT/Diodes used to transmit power from AC system 1 to AC system 2: AC system 1 is a 230 kV, 2000 MVA, 60 Hz system, having a Short Circuit Ratio (SCR) of 10 and consists of one source with an equivalent impedance $Z_{ac1} = 0.072 + j40.974\,\Omega$, length of ac cable is 50 km. AC system 2 is a 230 kV, 800

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MVA, 50 Hz system, having a SCR of 4 and consists of one source with an equivalent impedance $Z_{ac2} = 0.085 + j26.766\,\Omega$, length of AC cable is 50 km.

To simulate the system behaviour under parameters uncertainty conditions, faults are applied in cases A and B separately [10], as shown in Fig. 7. The Sinusoidal Pulse Width Modulation (SH-PWM) switching uses a two several triangular carrier signals with a frequency of 30 times fundamental frequency.

Case A:

t < 1.2 s, the system operates in normal conditions.

At t = 1.2 s, a single-phase to ground fault occurs at the transmission line 1.

At t = 1.3 s, line 1 is de-energized to clear the fault.

Case B:

t < 2.3 s, the system operates in normal conditions.

At t = 2.3 s, a three phase fault to ground occurs at the transmission line 2.

At t = 2.4 s, line 2 is de-energized to clear the fault.

Simulation results of system responses are shown in Figs. 8. First, figures 8.1. (a), (b) shows the magnitude seen from the bus bar where the filter is connected of the combined filter and AC network impedance as a function of frequency.

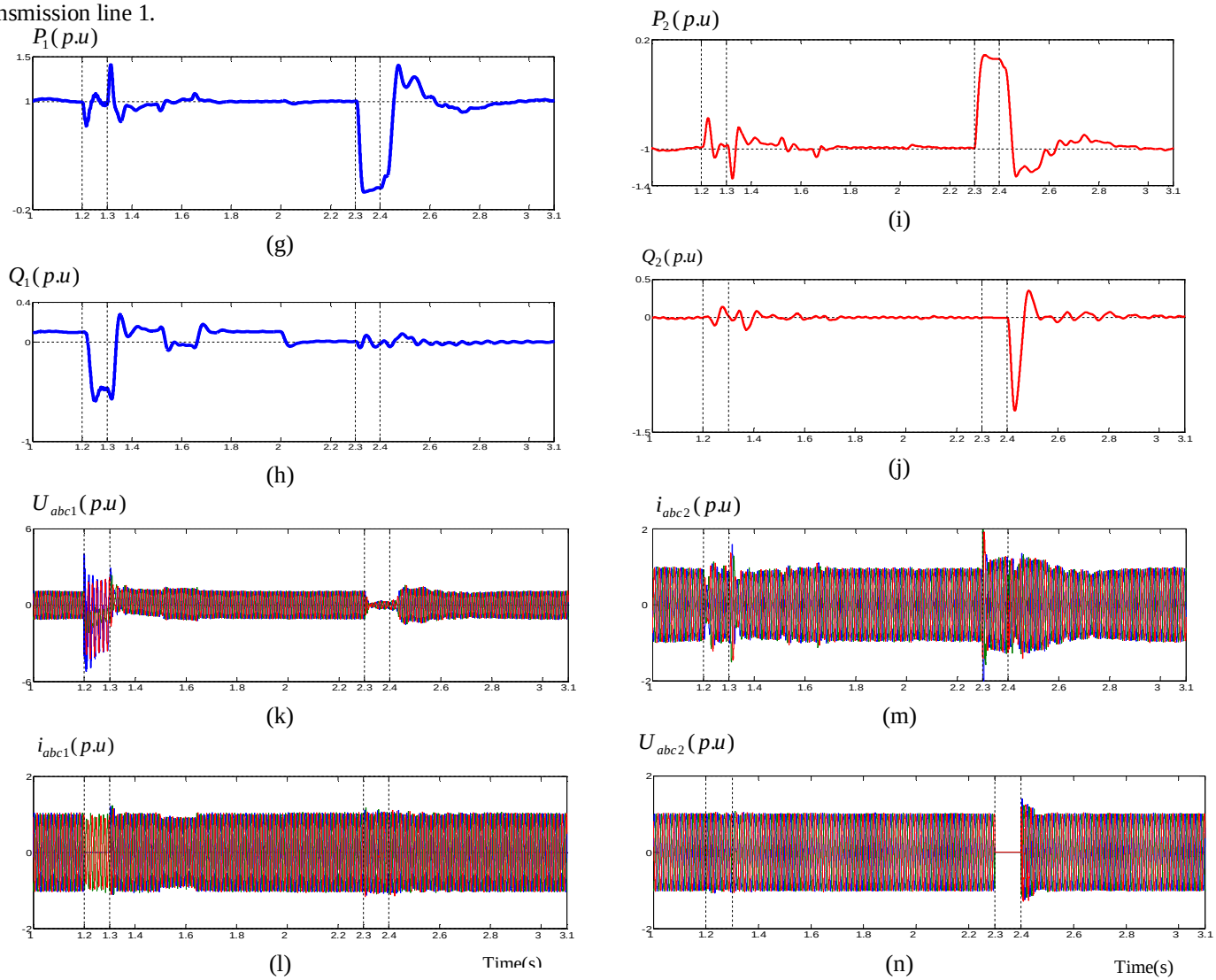

Fig. 8.3. ac side perturbations: (g)-(h) the transmitted active and reactive power at the Rectifier side.

(k)-(l)The transmitted active and reactive powers at the Inverter side (i)-(j) Rectifier ac phase current and Voltage. (m)-(n) Inverter ac phase current and Voltage.

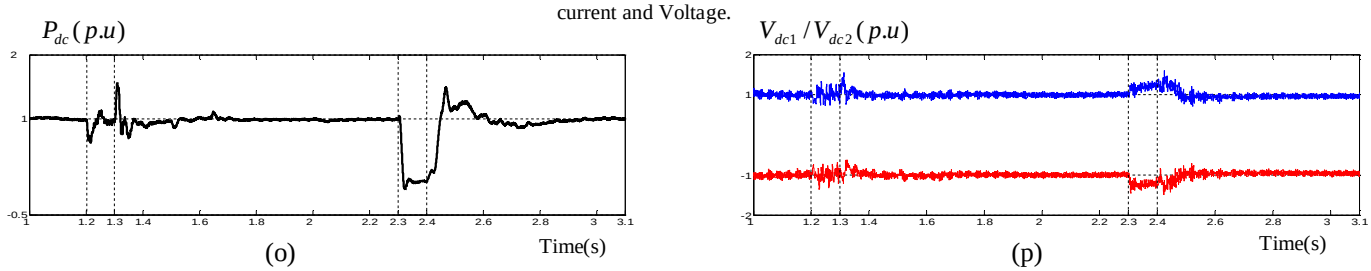

Fig. 8.4. (o) Active Power measured at the dc side. (p) dc voltages.

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Notice the two minimum impedances on the Z magnitudes of the ac systems: these series resonances are created by the 30th and 60th harmonic filters. They occur at 1800 Hz and 3200 Hz on the 60 Hz system (1500 Hz and 3000 Hz on the 50 Hz). The low principal natural frequency, coinciding with the parallel resonance at 257 Hz on the rectifier side and 216 Hz on the inverter side, is a determining factor in the development of the over voltages and interaction with the dc voltage [19].

is occurred at 1.2 s and 2.3 s that the current responses can quickly track the references. From fig 8.3.(g), (n) it can be seen that, when fault line 1 is de-energized in case A, the active power flow is 1 p.u, transmitted from VSC 1 to VSC 2 with same oscillation during the fault in case A. However, when faults occur at 2.3 s (case B), the transmitted power is reduced to 0 p.u and the values can return to the reference value after clearing the fault at 2.3 s after 0.5 s. the reactive power of VSC 1 decreased to 0.6 p.u during the fault at 1.2 s, with some oscillations at 2.3 s, when the reactive power of VSC 2 can track the reference in all operations, but we can see some oscillations after the severely fault at 2.3 s. Finally, the main dc and flying-capacitor voltages shows in fig 8.4 is maintained at the stable value 1 p.u with some oscillations during the fault in case A. During the fault in case B, the value progress about 1.1 pu, he recovers to the reference after 0.1s when the fault is cleared.

IV. Conclusion

A control system for an HVDC link with voltage sourced converters has been established in this paper. A mathematical model was developed in the synchronous reference frame. The mathematical model was then used to analyze and synthesize the voltage and current control loops for the VSC. The performance of the VSC-HVDC system was verified by balanced and unbalanced fault conditions. Simulation results show that with the proposed control strategy, rapid response and desirable stability have been reached for steady-state and dynamic conditions. In addition, it is also confirmed that the active and the reactive power can be controlled with no mutual interference.

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